CLAIMS

What is claimed is:

1. A method of fabricating a memory device having a core region including an array of double-bit memory cells and a periphery region including associated logic circuitry, said method comprising:

(a) providing a semiconductor substrate having a core area and a periphery area;

(b) forming a multi-layer dielectric stack over the substrate in the core area and in the periphery area;

(c) removing the multi-layer dielectric stack from the periphery area;

(d) forming at least one gate dielectric layer over the substrate in the periphery area;

(e) forming a first conductive layer over at least the periphery area;

(f) implanting ion species into the core area of the semiconductor substrate;

(g) performing a high temperature oxidation (HTO) step, said step being effective to (i) replace a top layer of the dielectric stack and (ii) activate implanted ion species to form buried bitlines in the core area;

(h) removing HTO from the periphery area; and

(i) forming a second conductive layer over the top layer of the dielectric stack in the core area and the first conductive layer in the periphery area.

2. The method according to claim 1, wherein the order of steps (d) through (f) is effective to minimize lateral diffusion of the implanted ion species.

3. The method according to claim 2, wherein the lateral diffusion of the implanted ion species forming the buried bitlines is no more than about 50 nanometers into an adjacent body region.

4. The method according to claim 1, wherein (i) replacing the top layer of the dielectric stack and (ii) activating implanted ion species to form buried bitlines in the core area are accomplished using a single thermal processing step.

5. The method according to claim 1, wherein the implanted ion species are subjected to no more than one thermal processing step.

6. The method according to claim 1, wherein the second conductive layer forms a gate electrode for the memory cells in the core area and the second and first conductive layers together form a gate electrode for the logic circuitry in the periphery area.

7. The method according to claim 6, wherein the first conductive layer has a thickness of about 500 angstroms to about 800 angstroms.

8. The method according to claim 7, wherein the second conductive layer has a thickness of about 900 angstroms to about 3,000 angstroms.

9. The method according to claim 1, wherein step (e) includes (i) forming the first conductive layer over the core area and the periphery area and (ii) removing at least the first conductive layer from the core area.

10. The method according to claim 1, wherein step (d) includes:

(i) growing a first gate oxide layer;

(ii) performing a first anneal cycle;

(iii) growing a second gate oxide layer over the first gate oxide layer; and

(iv) performing a second anneal cycle.

11. The method according to claim 10, wherein the first and second anneal cycles are each performed at a temperature of between about 600

degrees Celsius and about 1000 degrees Celsius for between about 15 minutes and about 60 minutes.

12. The method according to claim 1, wherein step (f) includes implanting ion species through a bottom dielectric layer and a charge trapping dielectric layer of the dielectric stack into the core area of the semiconductor substrate.

13. The method according to claim 1, wherein the multi-layer dielectric stack includes:

a bottom dielectric layer;

a charge trapping dielectric layer; and

a top dielectric layer.

14. The method according to claim 1, further comprising:

forming a plurality of isolation regions separating (i) the core region from the periphery region and (ii) adjacent logic circuitry devices in the periphery region.

15. The method according to claim 1, wherein step (a) includes doping the core area of the semiconductor substrate.

16. The method according to claim 1, wherein step (a) includes forming at least one of (i) high-voltage well implants and (ii) low-voltage well implants in the periphery area of the semiconductor substrate.

17. A charge trapping dielectric memory device fabricated according to the method of claim 1, wherein each double-bit memory cell in the core region includes a channel disposed between adjacent pairs of buried bitlines, said channels each having a length of about 1100 nanometers to about 1300 nanometers.

18. The charge trapping dielectric memory device according to claim 17, wherein each buried bitline has a lateral dimension of about 150 nanometers to about 200 nanometers.